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(54) Title of the Invention:

Insulated gate type semiconductor device

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SPECIFICATION

1. TITLE OF THE INVENTION

Insulated gate type semiconductor device

2. CLAIMS

1. An insulated gate type semiconductor device wherein a channel formation region of an insulated gate type field effect transistor comprises a non-single crystalline semiconductor added with hydrogen or a halogen element, a pair of impurity regions constituting a source and a drain neighboring said semiconductor has crystal growth promoted more than that of the semiconductor of said non-single crystalline semiconductor, and said regions having crystal growth promoted is provided penetrating in said channel formation region under the gate electrode.

2. The insulated gate type semiconductor device of Claim 1 wherein the channel formation region added with hydrogen or a halogen element at 1 atom% or more comprises a non-single crystalline semiconductor and a semiconductor with crystal growth promoted more than that of said non-single crystalline semiconductor.

3. DETAILED DESCRIPTION OF THE PRESENT INVENTION

"Field for Industrial Use"

The present invention relates to an insulated gate type field effect semiconductor device (hereinafter referred to as IGF) utilized for a semiconductor integrated circuit, a liquid crystal

display panel, etc.

"Prior Art"

An IGF utilizing single-crystalline silicon is widely utilized in the field of semiconductor. A typical example is Japanese Patent Pub. No. 50-1986 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor. When it comes to the IGF of which channel formation region not comprising a single-crystalline semiconductor but comprising a non-single crystalline semiconductor device added with hydrogen or a halogen element at 1 atom% or more, a typical example is shown in Japanese Pat. Appl. No. 53-124021 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor (filed on October 7, 1978).

This IGF of which channel formation region comprising a semiconductor especially a silicon semiconductor added with hydrogen or a halogen element, has off current of $1/10^3$ to $1/10^5$ compared with that of the conventional IGF utilizing a single-crystalline semiconductor. Therefore this is believed to be effective in use for an IGF for controlling a liquid crystal display panel.

As in the example above mentioned, there are three types of semiconductors as this IGF: there are a lateral channel type IGF wherein a gate electrode is formed on a semiconductor of a channel formation region, a vertical channel type IGF mentioned in Japanese Pat. Appli. No. 56-001767 "INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" (January 9, 1981), and a conventional thin film IGF transistor wherein a gate electrode is provided beneath a semiconductor composing a channel formation region. Compared with the latter two, the structure of the former is the same as that of the conventionally known IGF utilizing single-crystalline silicon. Thus this IGF has very good characteristic that a completed technology can be applied.

However, a source and a drain of this IGF should be formed not through a CVD method (including a plasma CVD method) by deposition of a thin film, but through ion implantation, etc. This additive should be made as active donor or acceptor through annealing at a temperature range of 400 °C or less in which hydrogen or a halogen element will not be deaired. In addition, improvement in reverse voltage proof in the source and the drain, especially between the drain and the channel formation region is demanded.

"Means to Solve the Problems"

The present invention is aimed at solving the problems above mentioned. A gate insulator is selectively formed on a non-single crystalline semiconductor (hereinafter non-single crystalline semiconductor added with hydrogen or a halogen element is simply referred to as semiconductor, or non-single crystalline semiconductor) to which no or little impurity has been added. On the gate insulator, a gate electrode is selectively provided.

With utilizing this gate electrode as a mask, impurities for the source and the drain are added by an ion implanting method or the like. For example, phosphorous or arsenic is added for N channel, and boron is added for P channel, into the non-single crystalline semiconductor to constitute impurity regions. After that, strong light is irradiated at 400 °C or less to the regions added with these inactive impurities. Strong light anneal (hereinafter simply referred to as light anneal) is performed. Thus a semiconductor with hydrogen or a halogen element added and resided, and with crystallization rate promoted more than the channel formation region is, is formed. Particularly, this semiconductor of the impurity regions is changed to a semiconductor with a polycrystalline or single-crystalline structure. Moreover, by extending this crystallization to the channel formation region, PI and NI junction

portions are made as portions with high crystallization rate.

In this manner, to improve voltage proof (to improve avalanche break down voltage) between the channel formation region and the junction portions, a polycrystalline or a single-crystalline region is provided near the PI or NI junction interface, said channel formation region being a non-single crystalline semiconductor added with hydrogen or a halogen element to decrease off current.

"Results"

As a result, in the structure of the IGF of the present invention, junction voltage proof of a source and a drain, especially of a drain can be made as high as that of a single-crystalline semiconductor. Compared with a thin film transistor including the conventional amorphous semiconductor, voltage proof is higher by nearly 20 V. In addition, a gate electrode is provided above a non-single crystalline semiconductor composing a channel formation region on a substrate. Impurity regions having optical Eg of 1.6 to 1.8 eV which is approximately the same as that of optical Eg (1.7 to 1.8 eV in the case of a silicon semiconductor) of this non-single crystalline semiconductor and being active are obtained. In this manner, as to "ON" and "OFF" of the IGF, because Eg is the same or approximately the same as that of the channel formation region, ON current is not difficult to flow at rise time. On the other hand, electric current is not subject to lazily flow at fall time. That is, off current is small, and ON, OFF can be performed in a high-speed response.

"Embodiment 1"

As is shown in Fig.1(A), a quartz glass substrate of 10 cm x 10 cm and 1.1 mm thickness is utilized as a substrate (1). A non-

single crystalline semiconductor(2) including amorphous structure added with hydrogen at a concentration of 1 atom% or more is formed at 0.2 μ thickness by a plasma CVD (high frequency of 13.56 MHz, substrate temperature of 210 °C) of silane (SiH_4). A silicon nitride film (3) is deposited as a gate insulating film by a photo CVD method on it. That is, Si_3N_4 is formed at 1000 Å thickness by reaction of Si_2H_6 and ammonia or hydrazine (low pressure mercury lamp at 2537 Å and substrate temperature of 250 °C) without utilizing mercury photosensitized method.

Then portions other than a region (5) composing an IGF is removed by a plasma etching method. This reaction is performed as CF_4 +O_2 (5%) at 13.56 MHz at a room temperature. A micro-crystalline or polycrystalline semiconductor of N^+ conductivity type is deposited at 0.3 μ thickness on this gate insulating film. This N^+ semiconductor film is removed utilizing a resist (6) by a photo etching method. Then phosphorous is added to the regions to be a source and a drain with utilizing this resist and N^+ semiconductor gate electrode portion (4) as a mask by an ion implanting method at a concentration of 1 x 10^{20} cm^{-3}, as is shown in Fig.1(B). Thus a pair of impurity regions (7) and (8) are formed.

After the resist of the gate electrode is removed from the whole substrate, strong light (10) annealing is performed. That is, light is irradiated in linear shape utilizing an extra-high pressure mercury lamp (output of 5 KW, wavelength of 250 to 600 nm, diameter of 15 mmϕ, length of 180 mm) backside of which is provided a parabolic reflection mirror, and in front of which is provided a quartz cylindrical lens (focal distance of 150 cm, converging width of 2 mm, length of 180 mm). The irradiated part of the substrate is scanned at a speed of 5 to 50 cm/min. to have strong light irradiated to the entire surface of the substrate of 10 cm x 10 cm.

Because a large amount of phosphorous has been added to the gate

electrode portion, this electrode absorbs light enough and is polycrystallized. The impurity regions (7) and (8) are once solved and recrystallized. Thus they are solved in the direction of scanning, that is, in the direction of X. Recrystallization is shifted (transported). As a result, compared with the case of heating or irradiating the entire substrate, grain size can be made bigger because a system of crystal grain growth has been added.

This region which has been polycrystallized reaches the entire peripheral region of the impurity regions. As is shown in the figure, the bottom of this polycrystallized region reaches even the substrate (1). As shown by broken lines (11) and (11'), the polycrystallized region plunges into junction interfaces (17), (17') of the impurity regions (7), (8), and is provided in the channel formation region at 0.3 to 3 μ thickness. Morphological interfaces (15) and (15') are provided under the gate electrode. That is, the ends (15) (15') are provided penetrating into the channel formation region transcending the ends of the gate electrode (16) (16'). Because N(7), (8) - I(2) junction interfaces (17) (17') are provided inside of the crystallized region, breakdown voltage becomes big to the reverse bias, and high voltage proof IGF can be formed. The crystallized semiconductor region in the I type semiconductor can be decided by scanning speed and intensity (irradiation) of light anneal.

In the figure, after the process in Fig.1(B), PIQ is coated on the whole surface at 2 μ thickness, and formed as electrode holes (13) (13'). Then ohmic contact of aluminum and its leads (14) (14') are formed. In the process of forming these (14) and (14') being a second layer, they can be connected with the gate electrode (4).

As a result of this light anneal, sheet resistance changed from 4×10^{-3} $(\Omega cm)^{-1}$ before light irradiation to $1 \times 10^{+2}$ $(\Omega cm)^{-1}$. This change in electric conductivity characteristic is clearly shown.

As is shown in Fig.2(21), drain voltage proof can be made not

less than 60 V in the case that the length of the channel formation region is 10 μ and the width of the channel is 1 mm. This is a condition when the gate voltage is situated V_{GG} = 10 V. This drain voltage proof is a great improvement compared with the case that the publicly known thin film transistor with junction region of amorphous structure has drain voltage proof varied widely from 30 to 50 V.

"Effects"

Because the present invention utilizes the manufacturing process of forming and processing films gradually from below, large-area large-scale integration is made real. Therefore IGF as many as 500 x 500 pieces can be formed in a 30 cm x 30 cm panel, and can be utilized as IGF for controlling a liquid crystal display device.

A semiconductor which has been polycrystallized or single-crystallized by light anneal process is extended to the channel formation region. As a result, the drain voltage proof is increased more than that of the conventional method, by 20 V or more.

As this light anneal utilizes ultraviolet rays, crystallization from the surface of the semiconductor to the portion inside is promoted. Thus electric current flowing through the channel formation region near the gate insulating film to the fully polycrystallized or single-crystallized impurity regions near the surface can be controlled with no problem.

Not any single-crystalline semiconductor is utilized as the substrate. Thus the portion inside of the channel formation region apart from the source, drain can keep non-single crystalline semiconductor condition without being influenced by the light irradiation anneal process. Therefore off current can be made $1/10^3$ to $1/10^4$ of that of a single-crystalline semiconductor.

Because the source and the drain are formed by light anneal

after formation of the gate, the interface with the gate insulator will not be dirty and its characteristic is stable. Not like the conventional method, not only quartz glass but also soda glass, a heat endurable organic film can be utilized at random as a substrate material.

In the present invention, process is performed in the same reaction chamber in which a semiconductor composing a channel formation region - gate insulator - gate electrode each of which being dissimilar interface are formed. Thus the semiconductor device of the present invention can be formed without being exposed to the air, and is characterized in that interface state is rarely generated.

In the present invention, it is preferable all impurity concentration of oxygen, carbon and nitrogen of non-single crystalline semiconductor of the channel formation region is 5×10^{18} cm^{-3} or less. In the conventionally known IGF, an impurity is contaminated in the channel layer at a concentration of 1 to 3×10^{20} cm^{-3}. In the case of utilizing an amorphous silicon semiconductor, life time of carriers, especially that of holes becomes short. Thus as a characteristic, current flown is as little as 1/3 or less of that of the present invention. In addition, hysteresis characteristic is observed when drain electric field is applied at 2×10^{6} V/cm or more to I_{DD} - V_{GG} characteristic. On the other hand, when oxygen is 5×10^{18} cm^{-3} or less, hysteresis is not confirmed even with an electric potential of 3×10^{6} V/cm.

4. BRIEF DESCRIPTION OF THE FIGURES

Fig.1 shows a cross sectional view of the manufacturing process of the insulated gate field effect semiconductor device of the present invention.

Fig.2 shows characteristic of drain current - drain voltage.

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